National Aeronautics and
Space Administration

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RADIATION EFFECTS IN MICROELECTRONICS— WHY WE NEED PARTICLE ACCELERATORS

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August 12, 2022

To be presented by J. Pellish at the 2022 North American Particle Accelerator Conference (NAPAC) in Albuquerque, NM on Aug. 12, 2022.

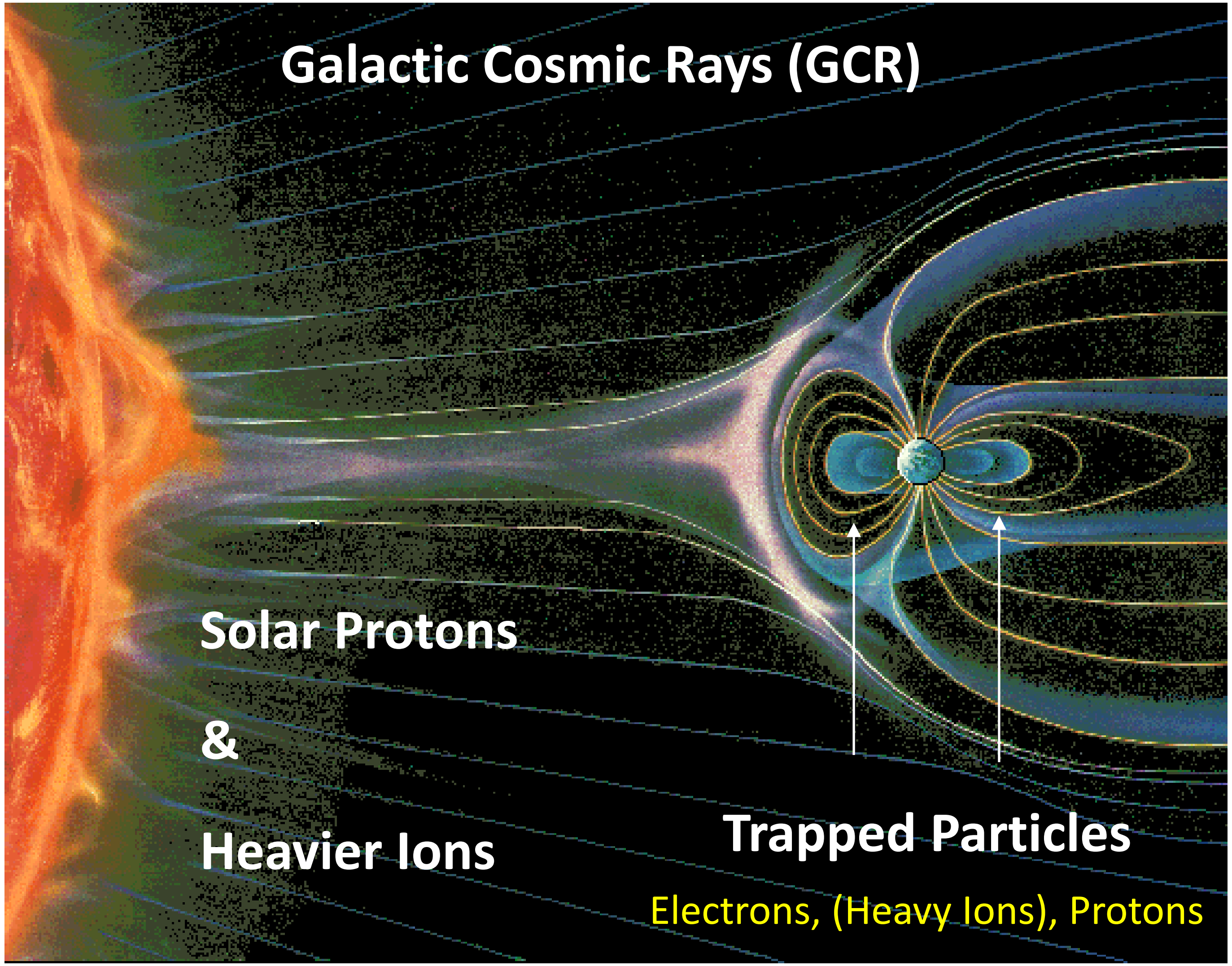
Outline

- ***Origins*** – what are single-event effects and why do we need to test?
- ***Evolution*** – how are test needs changing?
- ***Gaps*** – do we have access to sufficient capacity and necessary capabilities? (projecting ahead is hard)
- ***Mitigation*** – how do we overcome?

Talk will focus on heavy ion facilities in the United States
Large and diverse trade space – this is just one perspective
Test facilities are increasingly critical infrastructure for many economic sectors
…related topics can extend to proton and neutron test facilities too…

Natural Space Radiation Environment Near Earth

Dynamic



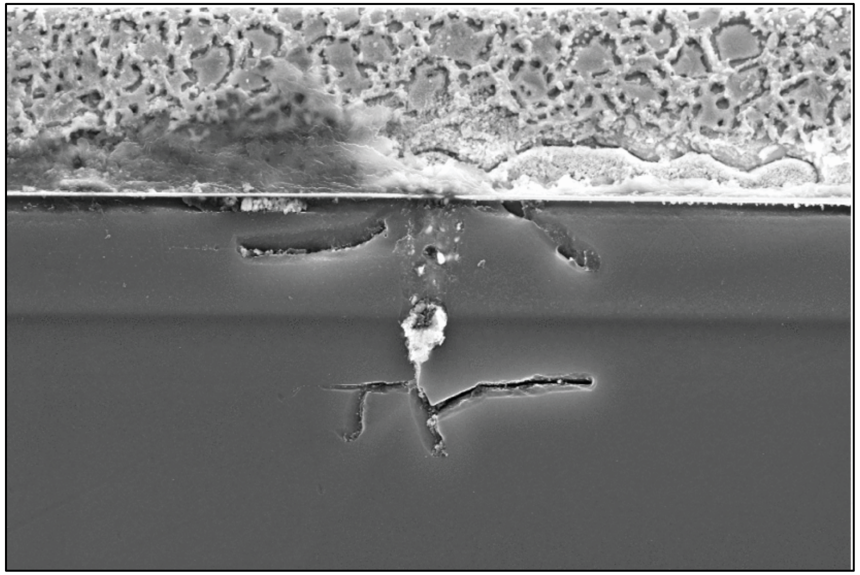
After J. Barth, *1997 IEEE NSREC Short Course;* K. Endo, *Nikkei Science Inc. of Japan;* and K. LaBel, *private communication.*

Spatio-temporal Variations

Single-Event Effects (SEE)

- SEE are any observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic-particle strike
- They can be destructive

Image of a SEE failure location in a Schottky diode



M.C. Casey *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, Jan. 2018

Halloween Storms (Oct 18 - Nov 7, 2003)

Courtesy of SOHO/LASCO consortium. SOHO is a project of international cooperation between ESA and NASA.

SEE History Timeline

1962 – SEE first postulated

- J.T. Wallmark & S.M. Marcus, "Minimum size and maximum packaging density of non-redundant semiconductor devices," *Proc. IRE*, vol. 50, pp. 286-298, Mar. 1962.

1975 – First satellite SEE anomalies reported

- D. Binder, E.C. Smith & A.B. Holman, "Satellite anomalies from galactic cosmic rays," *IEEE Trans. Nucl. Sci.*, vol. 22, no. 6, pp. 2675-2680, Dec. 1975.

1978/1979 – First observation of SEE on Earth

- T.C. May & M.H. Woods, "A New Physical Mechanism for Soft Errors in Dynamic Memories," *Int. Reliability Phys. Symp.*, Apr. 1978.
- J.F. Ziegler & W.A. Lanford, "Effect of Cosmic Rays on Computer Memories," *Science*, vol. 206, Nov. 1979.

1992 – First report of a destructive SEE in space

- L. Adams *et al.*, "A verified proton induced latch-up in space," in *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 1804-1808, Dec. 1992.

After S. Buchner, *2011 SERESSA Course*, Toulouse, France.

SEE Testing

- Why do we test?
  1. To determine the presence and characteristics of SEE
     - Destructive or non-destructive?
     - Voltage- and/or temperature-dependent?
     - *List goes on for a quite a while…*
  2. To calculate bounding SEE rates for a given mission, environment, application, and lifetime (“MEAL”) – this is what matters to designers, system engineers, etc.
- SEE testing is usually performed at particle accelerator facilities, which irradiate an electronic device target (or board or box) with ions
  - Neutrons, protons, heavy ions, or more exotic primaries

Typical SEE Test Hardware Setup

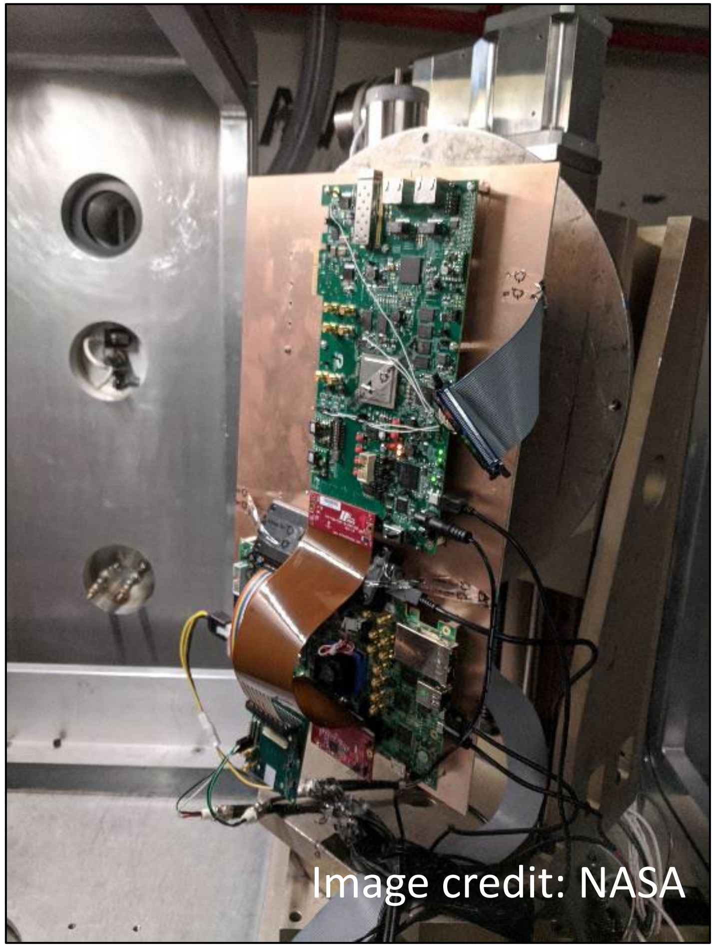


Image credit: NASA

Evolution

Technology Back Then…

Content and image courtesy of K. LaBel, SSAI Inc. / NASA GSFC, *Radiation Effects Boot Camp,* 2021.

- Devices were simple
  - Transistors
  - Memory arrays (4 kb SRAM!), 8-bit CPUs, etc.
  - High speed was 10 MHz operation
- Technologies were large and mostly silicon
  - >0.5 μm (some >2.0 μm) CMOS feature size
  - Gallium arsenide was emerging; rad-hard was silicon on sapphire
- Device packaging
  - Planar
  - Ceramic and a little plastic
  - Through-hole packages

650x Processor

- 8 μm feature size (not a typo) – ~1975
- 8-bit central processing unit
- Up to 14 MHz
- 64 kB random access memory
- 256 bytes stack
- No input/output ports
- 28 or 40-pin dual in-line package

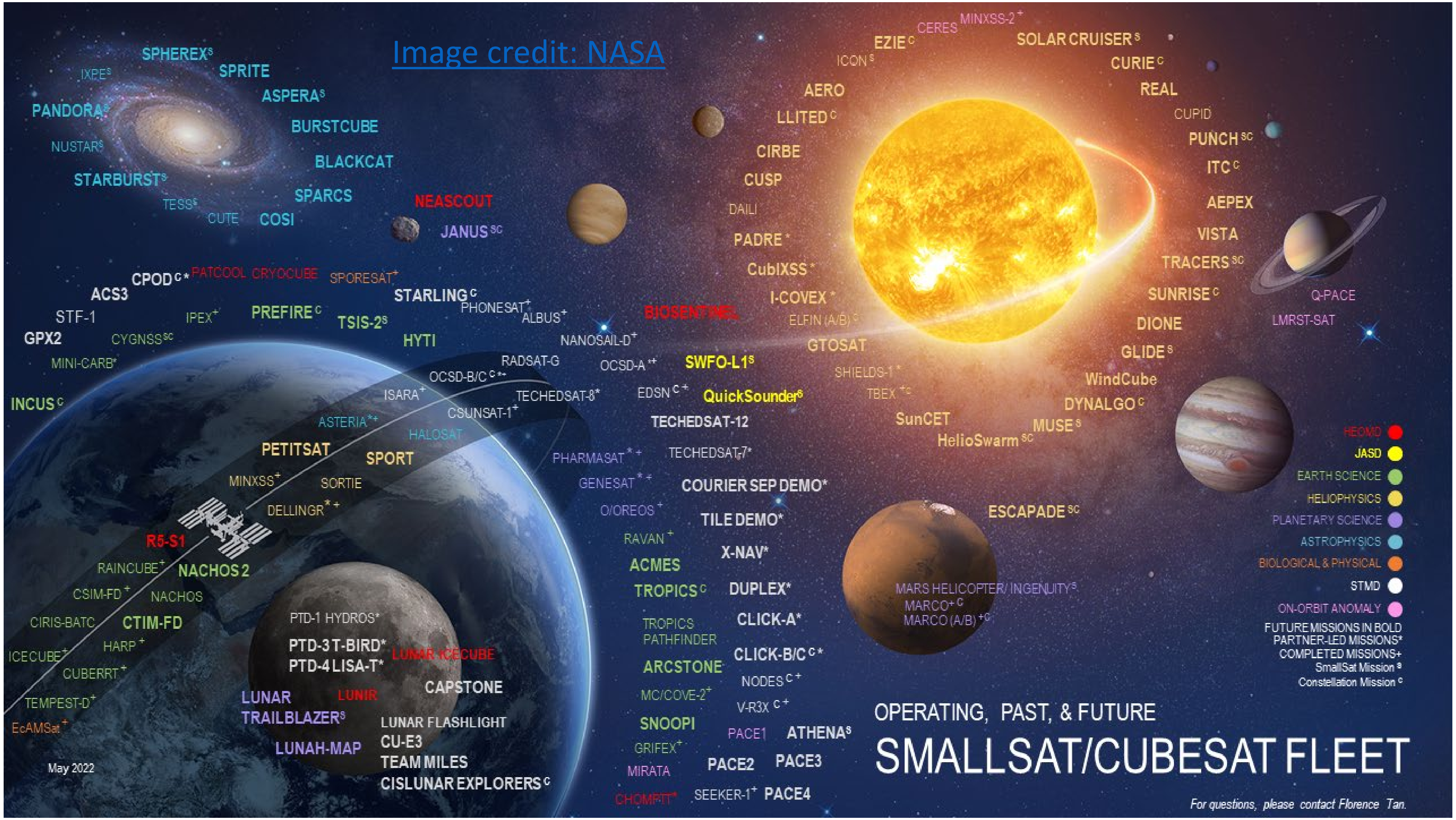
For SEE testing – it was easy to access to the die ("delidding") with limited SEE signatures (largely homogeneous devices)

…and Now

Content courtesy of K. LaBel, SSAI Inc. / NASA GSFC, *Radiation Effects Boot Camp,* 2021.

- Devices are not simple
  - Multi-core and heterogenous integration devices
  - >>Gbit Memories with built-in voltage conversion and microcontrollers
  - Extreme resolution or operating speeds and integration [*e.g.*, single devices replacing a whole card of devices from a decade or two earlier]
- Technologies aren't simple either
  - CMOS leading-edge feature size is <7 nm and soon <5 nm
  - Proliferation of wide bandgap (power and radio frequency devices)
  - Fins, gate all-around, and silicon-on-insulator are in!
    - Rad-hard = by design ("RHBD")
- Device packaging
  - Mix of planar (old school) and multi-dimensional (*i.e.*, 3D) packaging

User Community Growth and Diversification



User Community Growth and Diversification

Human Landing System

Commercial Crew Program

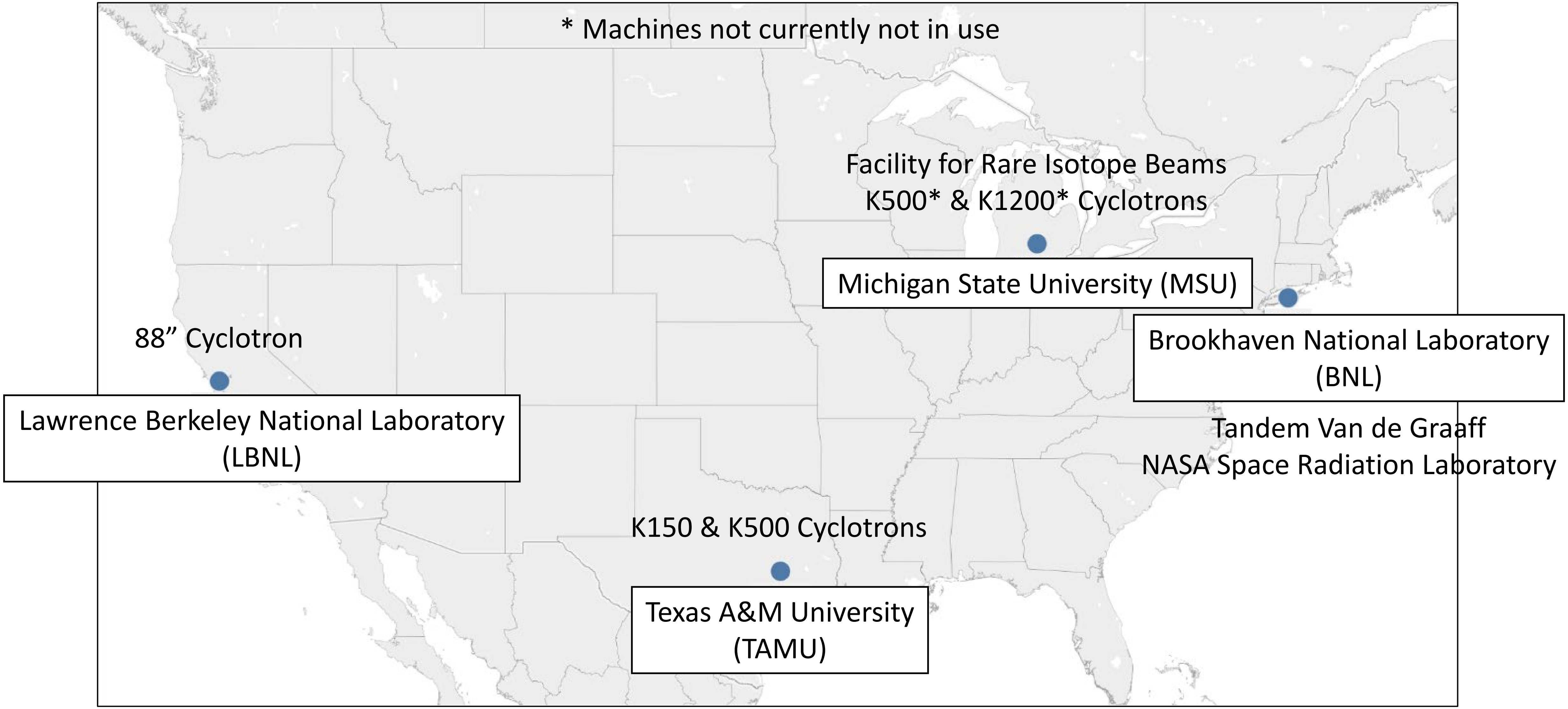
User Community Growth and Diversification

Image credit: The White House

- The CHIPS and Science Act of 2022 ([Public Law 117-167]), signed on Tuesday this week, will grow the U.S. microelectronics industry and likely have positive knock-on effects for radiation testing needs

Gaps

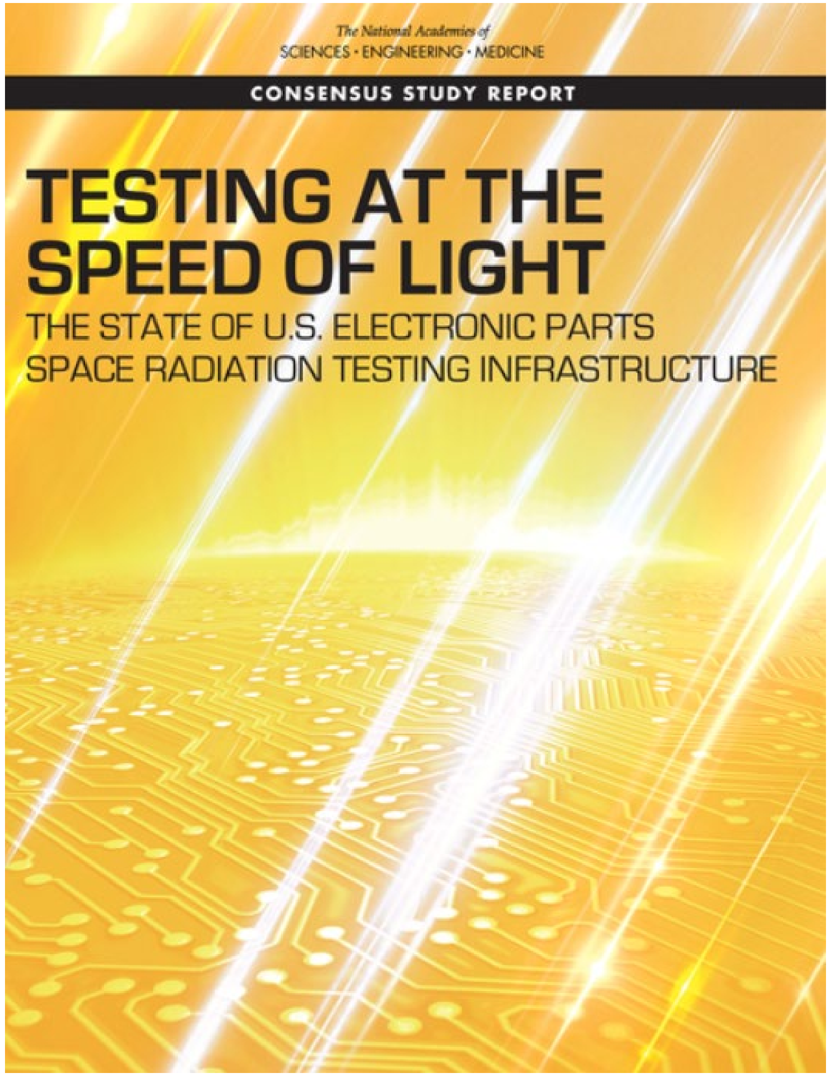
Major U.S. Heavy Ion SEE Test Facilities



Recent Assessments (National Academies 2017-2018)

- Key findings
  - Growing use and tightening supply
  - Infrastructure showing signs of strain
  - Aging workforce in a domain that requires specialized training and skills
  - Fast-moving technology
- Points to / needs
  - More organizational coordination
  - Test facility sustainment & new investments
    - Coupled with appropriate research & development
  - Workforce development

At least one detailed assessment pre-dated this work in the 2010s



https://doi.org/10.17226/24993

Recent Assessments—Analysis of Alternatives (AoA)

- Key findings from September 2020
  - Existing heavy ion SEE test facilities cannot meet current or future SEE test demand (~5000 hour/year gap)
  - Department of Defense efforts as well as U.S. Government and commercial space are driving significant increases in SEE testing demand
  - Current heavy ion accelerators for SEE testing at U.S. universities and Department of Energy labs have limited capacity and capability
  - More complex electronics (e.g., processors, ASICs, FPGAs) require more test hours
  - More advanced electronics and packaging (3D ICs, flip-chip packages, system-on-a-chip, or system-in-a-package) require higher ion energies >100MeV/n

Findings and Recommendations are
Independent and Non-Binding


Strategic Radiation-Hardened (SRH) Electronics Council (SRHEC) Public Summary from Analysis of Alternatives (AoA) for Domestic Single-Event Effects (SEE) Test Facilities

John Franco, DTRA
Jim Ross, NSWC Crane

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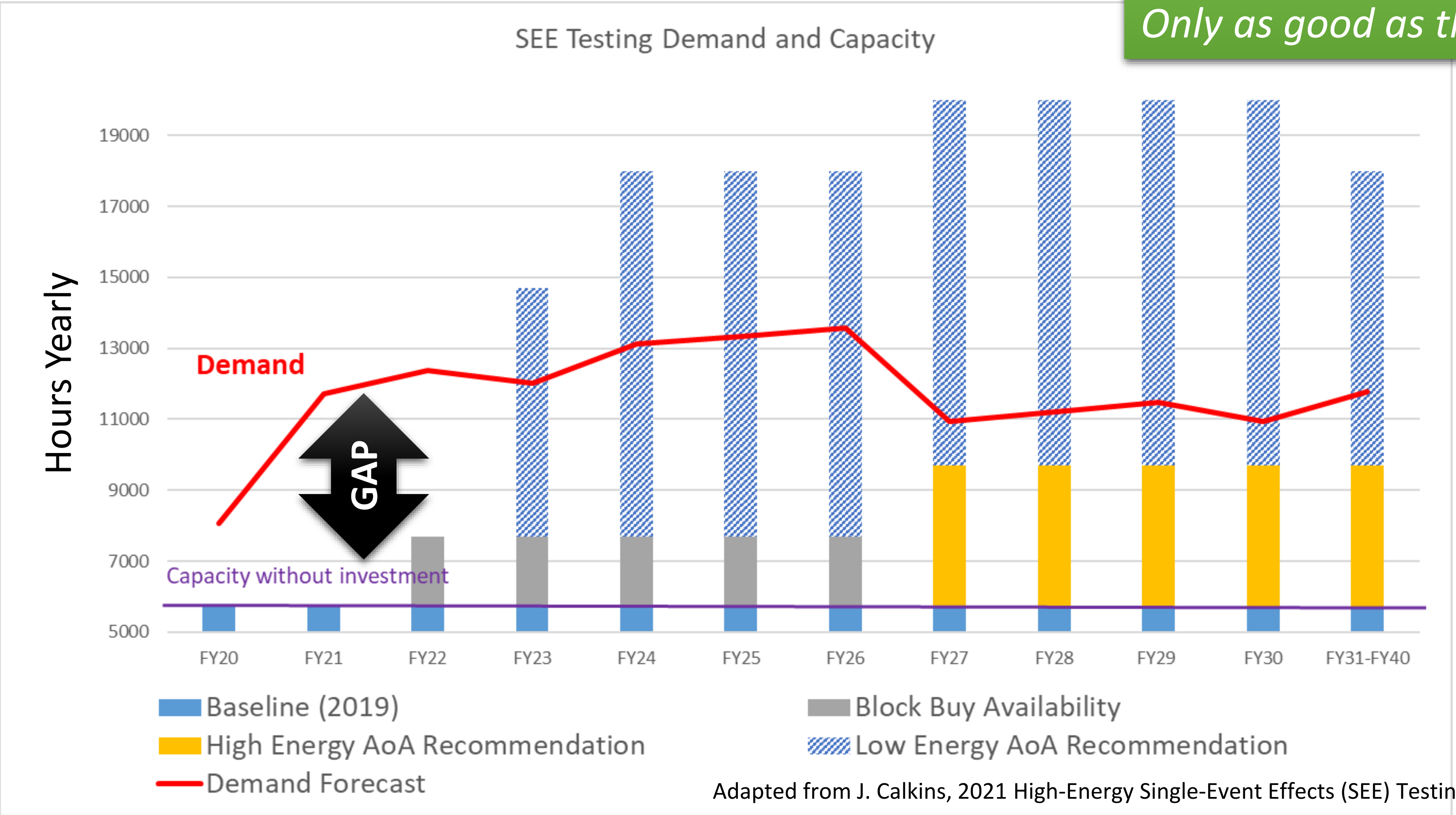
J. Calkins, 2021 High-Energy Single-Event Effects (SEE) Testing Users Meeting (slides)

Analysis of Alternatives (AoA)

Only a snapshot in time

Only as good as the data collected



Adapted from J. Calkins, 2021 High-Energy Single-Event Effects (SEE) Testing Users Meeting (slides)

Demand forecast is based on Fiscal Year 2020 projections of Defense programs (other contributors too!)
Demand input from integrators, manufacturers, and suppliers would improve fidelity of demand forecast

Analysis of Alternatives (AoA)

- Demand for high-energy SEE testing is growing (projections only)

Low Energy SEE Test

2020

- 90% of SEE test is Low Energy
  - 10-50 MeV/n (Mega-Electron Volts /n)

2030

- 60% of SEE test is Low Energy
  - Economical test for monolithic integrated circuits
  - Issues for flip-chip, stacked die, 2.5/3D packaging, and assemblies
- Access assured with low energy investments
- TAMU K500 & K150, LBNL, FRIB Lin Seg 1, and MSU K500 meet Low Energy demand

High Energy SEE Test

2020

- 10% of SEE test is High Energy
  - >100 MeV/n

2030

- 40% of SEE test is High Energy
  - New technology and CCA level testing will demand high energy
  - Economical for new technology
- Access assured by high energy investment
- 40% is ~4000 hours/yr
  - BNL AGS or MSU K1200 meets High Energy demand

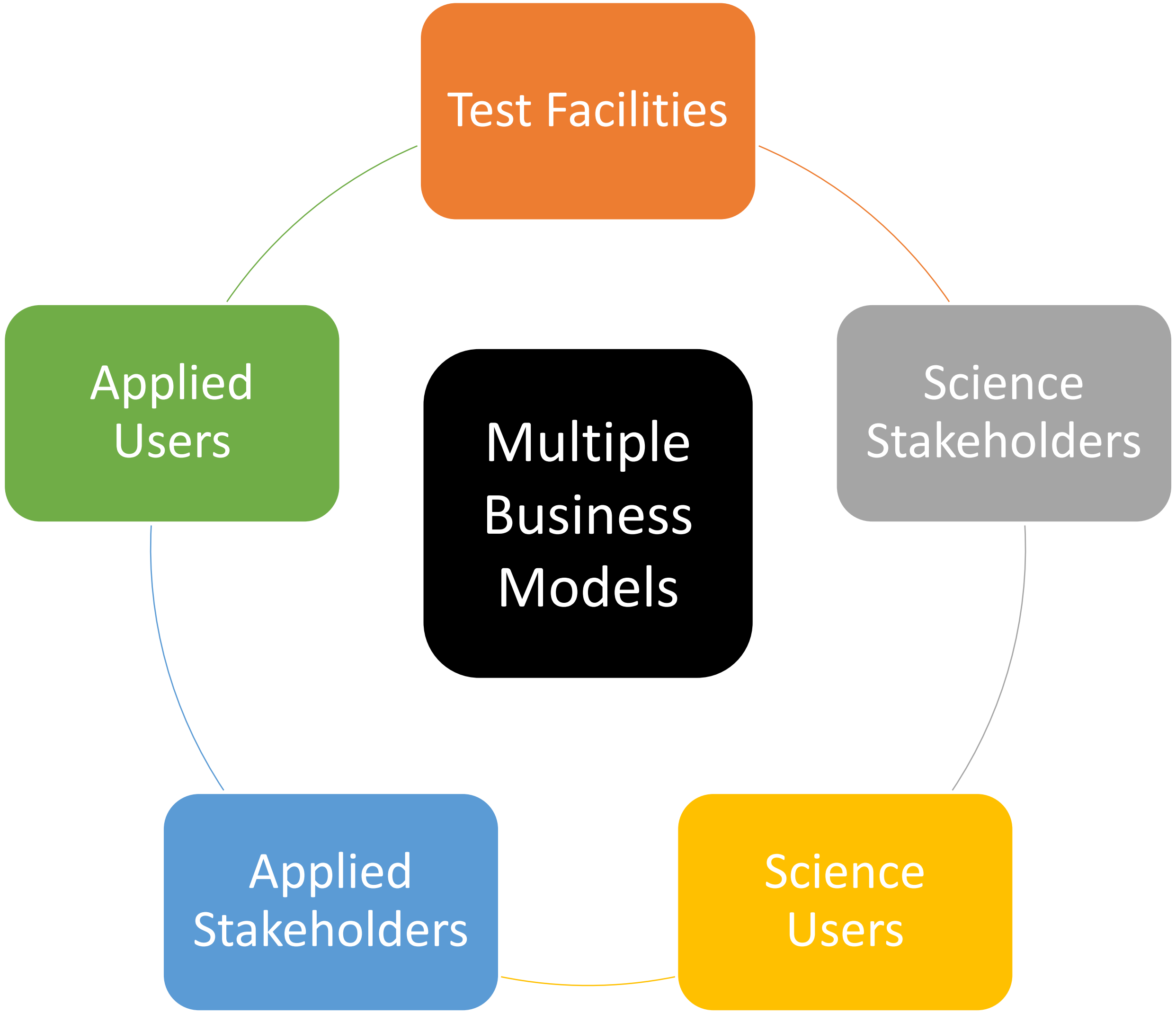
J. Calkins, 2021 High-Energy Single-Event Effects (SEE) Testing Users Meeting (slides)

Mitigation

More Organizational Coordination

Most facilities have multiple user and stakeholder communities

SEE testers are often guests in facilities designed and built for science



Need to invest in facilities is clear, but the trade space is complex

Unique time in the radiation effects community given planned investments & possibilities

Test Facility Sustainment & New Investments

- Utilize existing infrastructure to expand low-energy capacity
  - Repurpose available accelerator systems and leverage workforce, possibly gaining facilities dedicated to SEE testing
  - Consider reliability investment for current accelerator systems to increase availability through better efficiency and less downtime
  - *Needs are immediate and investments are happening*
- Continue and accelerate studies for new high-energy capabilities
  - Understand demand evolution for high-energy SEE – harder to predict, but know it is coming
    - Development and utilization phasing are stretched out relative to low-energy investments
    - Requires more funding up front (vs. low-energy) and *careful consideration of sustainable business models* for long-term operation
  - *Needs are growing and proposals are being considered*

Summary

- SEE testing is essential for robust space exploration, science, and commercial technology capabilities
- Testing infrastructure is an essential part of the U.S. industrial base
- Industry growth and expanding mission objectives are driving demand and have created gaps in both capacity and capabilities
- Mitigations exist and require sustained funding and coordination to execute successfully

- *While specifics may differ, these general themes appear outside the United States too*


NASA
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MOON LIGHTS THE WAY

Abbreviations

Abbreviation	Definition
3D	3-dimensional
AGS	Alternating Gradient Synchrotron
AoA	Analysis of Alternatives
ASIC	Application-Specific Integrated Circuit
BNL	Brookhaven National Laboratory
CCA	Circuit-Card Assembly
CHIPS	Creating Helpful Incentives to Produce Semiconductors
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
ESA	European Space Agency
FPGA	Field Programmable Gate Array
FRIB	Facility for Rare Isotope Beams
Gbit	1x10^9 bits (gigabit)
GCR	Galactic Cosmic Rays
IC	Integrated Circuit

Abbreviation	Definition
IEEE	Institute of Electrical and Electronics Engineers
LASCO	Large Angle and Spectrometric Coronagraph
LBNL	Lawrence Berkeley National Laboratory
MEAL	Mission, Environment, Application, and Lifetime
MSU	Michigan State University
NAPAC	North American Particle Accelerator Conference
NASA	National Aeronautics and Space Administration
NSREC	Nuclear and Space Radiation Effects Conference
RHBD	Radiation-Hardened By Design
SEE	Single-Event Effects
SOHO	Solar and Heliospheric Observatory
SRAM	Static Random Access Memory
SRH	Strategic Radiation-Hardened
SRHEC	Strategic Radiation-Hardened Electronics Council
TAMU	Texas A&M University