FRIB AND UEM LLRF CONTROLLER UPGRADE *

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Introduction

The tremendous discovery potential of FRIB can be further extended with an energy upgrade of the FRIB linear accelerator to 400 MeV/u and to higher energies for lighter ions. Footprint of the current (green and black) and upgraded (blue) FRIB linac.



Setup -

- Evaluation boards for ADC and DAC.
- Xilinx ZCU102 evaluation kit.
- ADC and DAC connected to ZCU102 via two high pin count FPGA mezzanine connector.
- Evaluation kits for power supply integrated chip and low noise amplifier.
- External band pass filter, low pass filter,



The low level radio frequency (LLRF) controller is designed to accommodate Facility for Rare Isotope Beams (FRIB) superconducting (SC) and Ultrafast Electron Microscope (UEM) room temperature (RT) cavity types (See Table 1).

	Table 1: Cav	vity Typ	es
System	Frequency (MHz)	Туре	Tuner
FRIB	40.25 - 322	SC/RT	Stepper/ Pneumatic
FRIB400	644	SC	Piezo/Stepper
UEM	1013.6	RT	N/A

The current LLRF controllers in operation at FRIB are based on Xilinx Spartan 6 field programmable gate array (FPGA) and support frequencies up to 322 MHz. With requirements for higher frequency operation there was a need to upgrade the LLRF controller. A comparison of current and new controllers is shown in Table 2.

Table 2: Controller comparison

Component	Current	New
Analog-to-Digital Converter (ADC)	TI ADS6442, 14-bit, 65 MSPS, 500 MHz bandwidth	TI ADS54J66, 14-bit, 500 MSPS, 900 MHz bandwidth
Digital-to-Analog Converter (DAC)	TI DAC5675A,14-bit, 400 MSPS	TI DAC37J82, 16-bit, 1.6 GSPS
FPGA	Xilinx Spartan-6	Xilinx Zynq Ultrascale Multi Processor System on Chip (MPSoC)
Phase Locked Loop (PLL) / Voltage Controlled Oscillator (VCO	TI LMK03000, Precision Clock Conditioner with Integrated VCO	TI LMK04828, Ultra Low- Noise JESD204B Compliant Clock Jitter Cleaner
RF Printed Circuit Board	FR4, 6 layer	RO4350B, 8 layer

splitter, frequency divider and attenuator.

Strategy -

• Proof of concept using evaluation kits done first to demonstrate capability of components identified for the upgrade.

Prototype

- Prototype RF front-end board was designed, fabricated and tested.
- The prototype RF board was redesigned with modifications and improvements for production.
- Given the low cost of Xilinx ZCU102, it was retained in the production version.

RF Input / Output

Input Non-IQ sampling -

- Higher order harmonics do not alias into baseband when sampled.
- Sampling frequency selected to digitally filter all harmonics.
- Mixing takes place after digitization
- Cascaded integrator-comb (CIC) filter suppresses harmonics.



Output Chain -

- Reduce number of components by using RF switch and band pass filters (BPF).
- Low pass filter (LPF) suppresses higher order harmonics and low noise amplifier (LNA) provides scaling of output.



CIC Filter Magnitude Response (dBc)

EPICS IOC

Running IOC server on the LLRF controller has many benefits including targeted maintenance, reduction in network traffic and latency, and distribution of resources.





LLRF Overview for TEST_LLRF:ZYNQ_N0002 5

RF Operation				de	Status	
	Setting	Readback	Cavity Phase Shift	154.2 °	Amplitude Mode	CW
Allow RF Operation	Allow		Cavity Detuning	1448.9 Hz	Feedback Status	Unlocked
RF Output	Enable Disable	Enabled			Regulate On	Cavity Pick-up Antenna
Auto Restart	Start Pause	Disabled	-Self-Excited Loop Mo	de	Set-Point Ramping	At Set-Point
Beam Tuning Mode	Enable Disable	Disabled	Loop Detuning	-0.0 Hz	Turne	
-Setpoints			Detuning Average	-0	_ uner	
Corponito	Setting Readb	ack Real-Time			Stepper Position	0 Reset

New LLRF Controller Chassis



Components -1. Xilinx ZCU102 FPGA Board

- 2. RF Board
- 3. Piezo Tuner
- board
 4. 1U Switching Power Supply
 5. 2.5-inch Solid State Drive

Features –2U chassis

- Efficient thermal design with multiple cooling fans
- Single power supply for all components
- Rack mountable
- Modular

Amplitude	2.5000 MV/m	2.5000 MV/m	2.5000 MV/m	RF Inputs-					
Phase	0.0 °	0.0 °	0.0 °		Amplitude	Phase	Power	Electric Field	
				Forward	0.3450 Vp	154.3 °	0.0 W		
-Feedback Mode	Catting			Reflected	0.3331 Vp	85.5 °	0.0 W		
Annality of Frankson	Setting		кеадраск	Cavity	0.3885 Vp	0.0 °	0.0 W	0.3885 MV/m	
Amplitude Feedback	ADRC						1		
Phase Feedback	Phase Feedback ADRC ADRC								
Tuner Feedback	On Off Oisabled			la ta al a al a	Feedback Performance				
Control Parameters	Control Parameters		-Interlocks	Statu	s	MS Amplitude Error	05.1		
Feedforward Phase 10 🔺 10.0 °			Latch	ed	twis Amplitude Error	00-1			
		Programmable Logic C	Programmable Logic ControllerImage: OKPersonnel Protection SystemImage: OK		RMS Phase Error	1E-3 *			
		Personnel Protection S				Statistics			
Cavity Conditioning	ing Cavity Conditioning		Machine Protection Sy	stem 🔘 OK					
Hardware Calibration	ibration Calibration		PLL Unlocked	🧿 ок					
Input/Output Attenuation	n Attenuation		Solid State Amplifier Fa	ault 🧿 <mark>OK</mark>					
System Configuration	tion System Configuration		Sum Status	💿 ок					
System Information	System Information		Reset Latched Interloc	Reset Latched Interlocks Reset					
		Detail and	Detail and Configuration						



Facility for Rare Isotope Beams

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