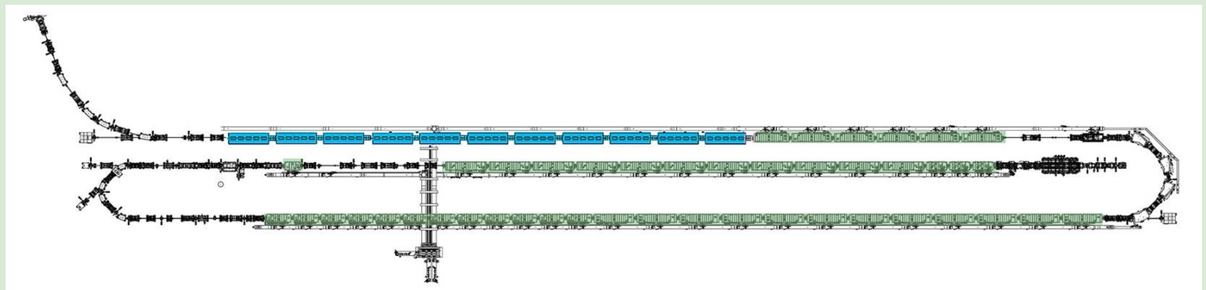
FRIB AND UEM LLRF CONTROLLER UPGRADE *

Shriraj Kunjir (kunjir@frib.msu.edu), E. Bernal, D. Morris, S. Zhao, FRIB, Michigan State University, East Lansing, MI 48824, USA
C-Y. Ruan, Department of Physics and Astronomy, Michigan State University, East Lansing, MI, 48824, USA

Introduction

The tremendous discovery potential of FRIB can be further extended with an energy upgrade of the FRIB linear accelerator to 400 MeV/u and to higher energies for lighter ions. Footprint of the current (green and black) and upgraded (blue) FRIB linac.



The low level radio frequency (LLRF) controller is designed to accommodate Facility for Rare Isotope Beams (FRIB) superconducting (SC) and Ultrafast Electron Microscope (UEM) room temperature (RT) cavity types (See Table 1).

Table 1: Cavity Types

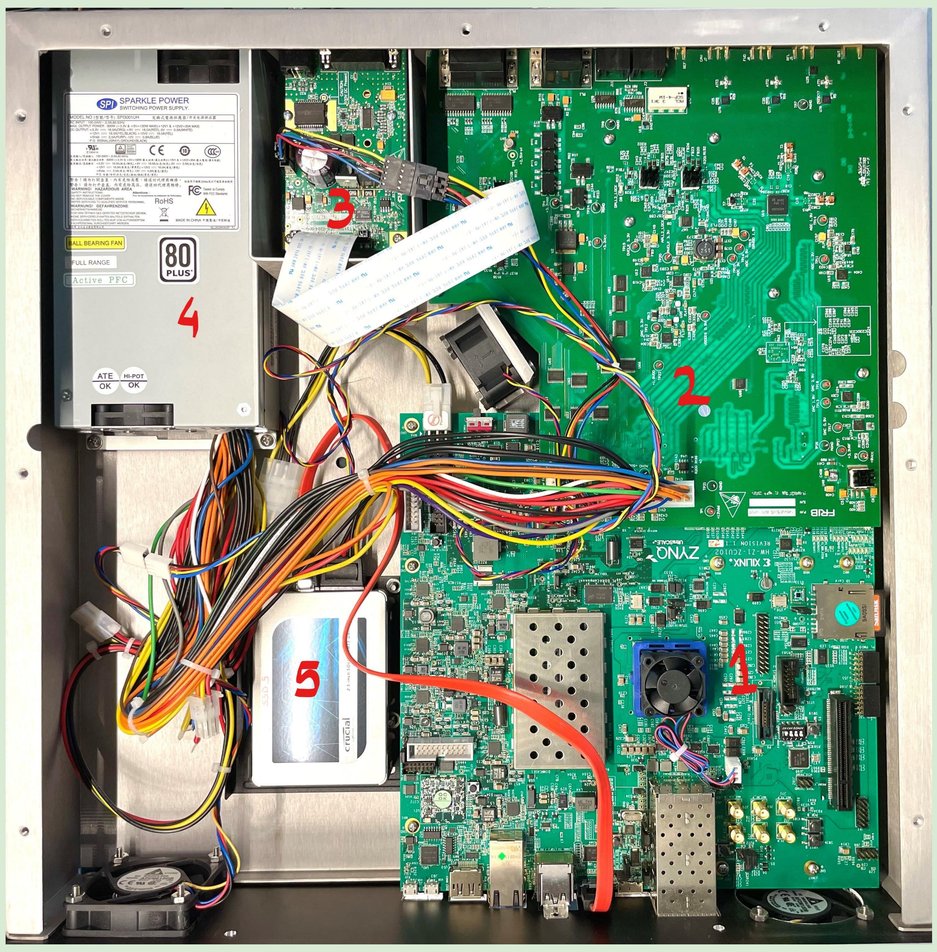
System	Frequency (MHz)	Type	Tuner
FRIB	40.25 - 322	SC/RT	Stepper/ Pneumatic
FRIB400	644	SC	Piezo/Stepper
UEM	1013.6	RT	N/A

The current LLRF controllers in operation at FRIB are based on Xilinx Spartan 6 field programmable gate array (FPGA) and support frequencies up to 322 MHz. With requirements for higher frequency operation there was a need to upgrade the LLRF controller. A comparison of current and new controllers is shown in Table 2.

Table 2: Controller comparison

Component	Current	New
Analog-to-Digital Converter (ADC)	TI ADS6442, 14-bit, 65 MSPS, 500 MHz bandwidth	TI ADS54J66, 14-bit, 500 MSPS, 900 MHz bandwidth
Digital-to-Analog Converter (DAC)	TI DAC5675A,14-bit, 400 MSPS	TI DAC37J82, 16-bit, 1.6 GSPS
FPGA	Xilinx Spartan-6	Xilinx Zynq Ultrascale Multi Processor System on Chip (MPSoC)
Phase Locked Loop (PLL) / Voltage Controlled Oscillator (VCO	TI LMK03000, Precision Clock Conditioner with Integrated VCO	TI LMK04828, Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner
RF Printed Circuit Board	FR4, 6 layer	RO4350B, 8 layer

New LLRF Controller Chassis

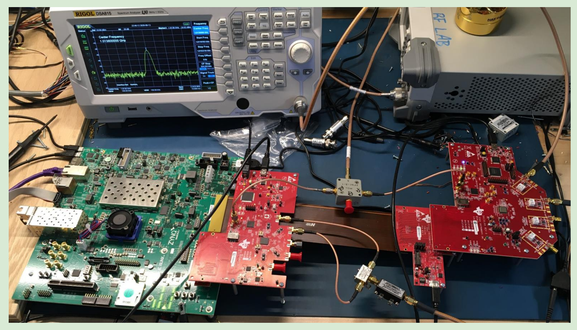


Components -
1. Xilinx ZCU102 FPGA Board
2. RF Board
3. Piezo Tuner board
4. 1U Switching Power Supply
5. 2.5-inch Solid State Drive

Features –
- 2U chassis
- Efficient thermal design with multiple cooling fans
- Single power supply for all components
- Rack mountable
- Modular

Prototype

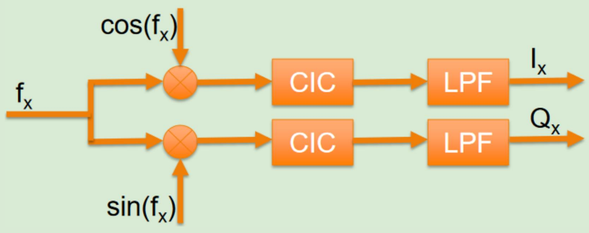
Setup -
- Evaluation boards for ADC and DAC.
- Xilinx ZCU102 evaluation kit.
- ADC and DAC connected to ZCU102 via two high pin count FPGA mezzanine connector.
- Evaluation kits for power supply integrated chip and low noise amplifier.
- External band pass filter, low pass filter, splitter, frequency divider and attenuator.

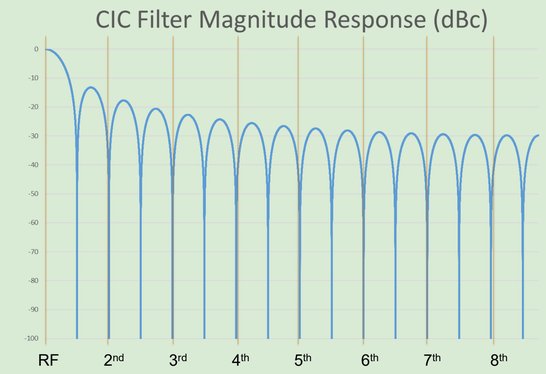


Strategy -
- Proof of concept using evaluation kits done first to demonstrate capability of components identified for the upgrade.
- Prototype RF front-end board was designed, fabricated and tested.
- The prototype RF board was redesigned with modifications and improvements for production.
- Given the low cost of Xilinx ZCU102, it was retained in the production version.

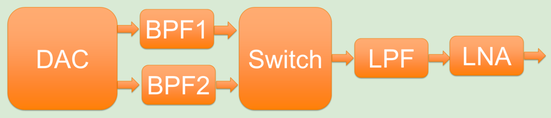
RF Input / Output

Input Non-IQ sampling -
- Higher order harmonics do not alias into baseband when sampled.
- Sampling frequency selected to digitally filter all harmonics.
- Mixing takes place after digitization
- Cascaded integrator-comb (CIC) filter suppresses harmonics.



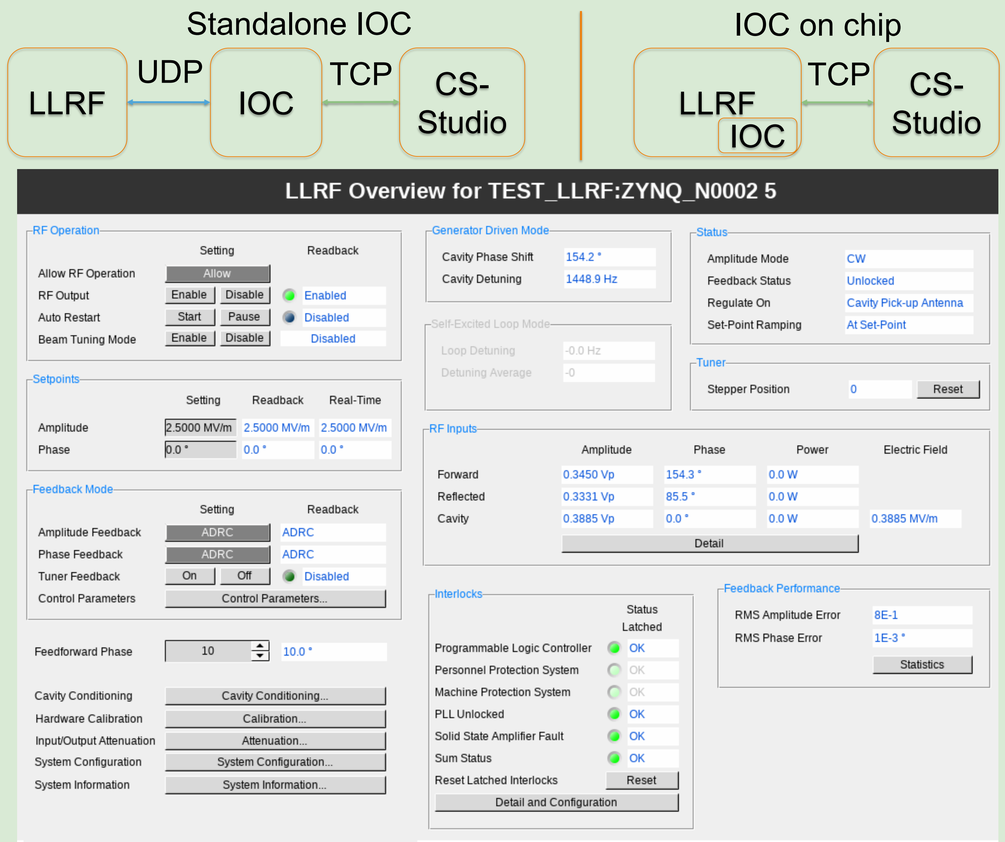


Output Chain -
- Reduce number of components by using RF switch and band pass filters (BPF).
- Low pass filter (LPF) suppresses higher order harmonics and low noise amplifier (LNA) provides scaling of output.



EPICS IOC

Running IOC server on the LLRF controller has many benefits including targeted maintenance, reduction in network traffic and latency, and distribution of resources.



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